REMARKS

The Office Action mailed June 30, 2005 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Subject Matter Indicated Allowed or Allowable

Applicants gratefully acknowledge the indication of allowable subject matter in claims 38 and 50, subject to their re-writing in independent form. Claims 38 and 50 have been rewritten in independent form to include the limitations of independent and intervening claims.

Rejection(s) Under 35 U.S.C. § 103 (a)

Claims 36, 37, 39, 40, 44 - 49, 51 and 52 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Diorio et al. (U.S. Pat. No. 5,990,512) in view of Alavi et al. (U.S. Pat. No. 5,844,300).

According to the Manual of Patent Examining Procedure (M.P.E.P.),

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.[1]

According to the Office Action:

> "In regard to claims 36 and 44 - 48, Diorio et al. teach a PFET synapse transistor and p-channel floating gate device 32, comprising: a p-doped substrate' (sic), a first n- well (left well) and a second n- well (right well) disposed in the substrate; a first p+ doped region disposed in the first n- well (left well) forming a

[1] M.P.E.P § 2143.

source (left p+ region) and a second p+ doped region disposed in the first n- well (left well) forming a drain (right p+ regional (sic); a channel disposed in the first n-well (left well) between the source (left p+ region) and the drain (right p+ region); a tunneling junction in the second n- well (right well); a layer of gate oxide 50 disposed above the channel, the first n- well (left well) and the second n-well (right well; a polysilicon floating gate 44 disposed above the layer of gate oxide 50; a source contact terminal electrically coupled to the source (left p+ regional (sic); a drain contact terminal electrically coupled to the drain (right p+ regional (sic); a well contact terminal coupled to the second n- well (right well) (Figures 7A-7B, columns 10 - 11, lines 37 - 67 and 1 - 30, respectively).

"In regard to claim 44 concerning the synapse transistor configured to operate as a current source without gate input using a single polysilicon gate layer, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 14 USPQ2d 1525, 1528 (Fed. Cir. 1990).

"In regard to the preamble of claims 45 and 47, the body of the claims is taught by the applied reference.

"In regard to claims 39 and 51, Diorio et al. teach the transistor formed with a single layer of conductive polysilicon 44 (Figures 7A-7B, columns 10 - 11, lines 37 - 67 and 1 - 30 respectively).

"However, Diorio et al. fail to teach a third p+ doped region and a fourth p+ doped region disposed in a second well.

"In regard to claim 36, Alavi et al. teach a third p+ doped region and a fourth p+ (Figure 3, column 4, lines 40 - 67).

"Since Diorio et al. and Alavi et al. are from the same field of endeavor (PFET transistors), the purpose disclosed by Alavi et al. would have been recognized in the pertinent art of Diorio et al.

"Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the PFET synapse transistor structure as taught by Diorio et al. with the structure having third and fourth p+ doped regions disposed in a second well as taught by Alavi et al. to provide a single polysilicon device (title and col. 1, lines 46 - 54).

> "In regard to claims 37 and 49, Alavi et al. teach the third p+ doped region and the fourth doped region disposed in a second well 41 p+ doped region (in n- well 41) shorted together with a conductive layer 60 which forms a bridge over a floating gate (Figure 3, columns 4 - 5, lines 40 - 67 and 17 - 25, respectively).
>
> "In regard to claim 40, Alavi et al. teach the transistor fabricated using a CMOS process. Also, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorne et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP §2113.
>
> "In regard to claim 52, Alavi et al. teach fabricating using a standard CMOS process (column 1, lines 46 - 54)."

As pointed out in response to the last office action/advisory action, Applicants' position is that the two cited references—Diorio et al. and Alavi et al.—are incompatible with each other, and therefore cannot be properly combined in an obviousness rejection under 35 U.S.C. § 103(a). That discussion is reincorporated herein by reference as if set forth fully herein. While this Office Action withdraws the prior rejection without explanation except for imposing a nearly identical rejection in its place, no attempt has been made by the Examiner to refute the basis of Applicants' argument, that is, that the references are incompatible with one another and it would not make sense for one of ordinary skill in the art at the time the invention was made to draw a suggestion for combination of bits and pieces of these references to form the claimed invention.

Accordingly, the Office Action is simply engaging in the prohibited practice of hindsight reconstruction.

Alavi et al. is directed to a semiconductor device used in the process of fabrication to measure accumulated charge. The portion of Alavi et al. supposed to coincide with the structure of the second n- well and the structure disposed therein in accordance with the presently claimed invention constitutes a capacitor wherein the two p+ regions are always shorted together and, in accordance with Alavi et al, to an antenna structure for acquiring charge during a fabrication step. This is true of the structure associated with n- wells 21 and 22 of FIG. 2, n- wells 41 and 42 of FIG. 3, n- wells 41 and 42 of FIG. 4, n- wells 41 and 42 of FIG. 5.

Alavi et al. does not suggest that ONE of its capacitor devices should be used alone nor does it suggest that its capacitor devices should be separated from their respective antenna charge collectors. NOR does it teach how to use these structures in connection with some application other than fabrication of semiconductors and measurement of stray charge collected during such fabrication. To combine Alavi et al. with Diorio et al. would therefore necessarily mean including BOTH of the shorted capacitor structures of Alavi et al. into the structure of Diorio et al. This would leave the resulting device inoperable because Diorio et al's device utilizes relative biasing of the p+ regions of the first n- well to inject electrons onto the floating gate of the injection transistor. Alavi et al. shorts the regions which might be considered a "source" and a "drain" and couples them to an antenna. The presence of such an antenna would disrupt the operation of the presently claimed invention as control of the present invention is not described in the specification to be under the control of random external charge flux.

To make it absolutely clear, voltages applied to the drain and source of the injection transistor are controlled so as to be able to form a channel (explicitly included in the limitations of the above-cited claims) and cause corresponding charge injection. Similarly voltages applied

to the tunneling structure are applied to cause certain desired charge transfer effects. Alavi et al's device lacks a channel and has no injection transistor. It operates by creating a relative bias between the floating gate and the tied-together p+ regions (also tied to an antenna device to obtain charge). Without its antenna it would be completely useless as there would be no way to put charge on the floating gate. With its antenna it is subject to control by random external charge flux which may be useful in the context of a monitoring device in a manufacturing process but is not otherwise desirable.

Accordingly, the two devices cannot simply be combined together to yield the claimed subject matter and one of ordinary skill in the art at the time the invention was made would not have taken portions of the capacitor charge-reception structures of Alavi et al. to use them with Diorio et al. so as to replace Diorio et al's FIG. 7B F-N tunneling junction with PART of Alavi et al's capacitor/antenna charge capture structure. There is certainly no suggestion in the art cited by the Office Action to that effect.

There is no suggestion to combine, accordingly, the claims are allowable.

Objected-To Claims

Claims 38 and 50 stand objected to as being dependent upon a rejected base claim but allowable if rewritten in independent form including all of the limitations of the rejected base claim and any intervening claims.

Claims 38 and 50 have been so rewritten and are, therefore, now allowable.

Claims Dependent Upon Objected-To Claims

Claim 39 is dependent upon allowable Claim 38 and claim 51 is dependent upon allowable claim 50, according these claims are also allowable.

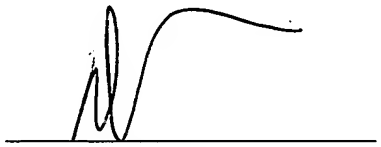
Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.



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